UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
FLANDERS, ANDREW C

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2000*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-13* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☒ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1.   Claim 7 objected to under 37 CFR 1.75(c) as being in improper form because a

multiple dependent claim cannot depend from any other multiple dependent claim (i.e.

claim 3). See MPEP § 608.01(n). Accordingly, the claim has not been further treated

on the merits.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1 – 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Sousa (European Patent Application 0 564 089 A1) in view of Uramoto (European

Patent Application 0 506 111 A2).

4.   Regarding Claims 1 and 11, Sousa discloses a method of decoding digital audio

data (page 2, lines 11-13), a step of obtaining an input sequence of data elements

representing encoded audio samples (page 6 lines 51 – 53), preprocessing the input

sequence of data elements (page 17 lines 32 – 39 and fig 12), performing a modified

discrete cosine transform (abstract) and forming decoded audio signals (page 17 lines

32 – 39). Sousa does not disclose the way the processing of the input data is

performed. Uramoto disclose a data processing method for video data (page 8, lines 15

– 37 and fig 5), method steps of calculating an array of sum data (page 8 lines 27 – 30),

an array of difference data (page 8 line 31), calculating a first sequence of output values

using the array of sum data (page 8 lines 32 – 37), calculating a second sequence of

output values using the array of difference data (page 8 lines 32 – 37). It would have

been obvious to one of ordinary skill in the art at the time of the invention namely when

the same result is to be achieved; i.e. to reduce the amount of processing required for

decoding, to apply the features of Uramoto to Sousa thereby arriving at a method

according to claim 1.

5.   Regarding Claim 2, in addition to the elements stated above regarding claim 1,

Uramoto further discloses the input circuit receives sequentially output sets of data (x0,

x7) and then adder 22 adds the data i.e. (x0 + x7) (page 8 lines 27 – 29) (i.e. wherein

the array of sum data is obtained by adding together respective first and second data

elements from the input sequence, the first and second data elements being selected

from mutually exclusive sub-sequences of the input sequence).

6.   Regarding Claim 3, in addition to the elements stated above regarding claims 1

and 2, Uramoto further disclose the input circuit receives sequentially output sets of

data (x0, x7) and then subtractor 23 subtracts the data (x0 – x7) (page 8 lines 27 – 31)

(i.e. wherein the array of difference data is obtained by subtracting respective first data

elements from corresponding second data elements of the input sequence, the first and

second data elements being selected from mutually exclusive subsequences of the

input sequence).

7.   Regarding Claim 4, in addition to the elements stated above regarding claim 1,

Uramoto discloses dividing X into (x0, x7), the first and last elements of X (page 8 lines

27 – 28) (i.e. wherein the step of calculating an array of sum data and an array of

difference data comprises dividing the input data sequence into first and second equal

sized sub-sequences, the first sub-sequence comprising the higher order data elements

of the input sequence and the second sub-sequence comprising the low order data

elements of the input sequence), adder 22 adds the data i.e. (x0 + x7) (page 8 lines 27

– 29) (i.e. calculating the array of sum data by adding together each respective data

element of the first subsequence with a respective corresponding data element of the

second sub-sequence) and then subtractor 23 subtracts the data (x0 – x7) (page 8 lines

27 – 31) (i.e. and calculating the array of difference data by subtracting each respective

data element of the first sub-sequence from a respective corresponding data element of

the second sub-sequence).

8.   Regarding Claim 5, in addition to the elements stated above regarding claim 1,

the output of the addition and subtraction (fig. 5 element 500) is applied to a data

rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output

is then applied to a product sum operation circuit (fig. 8 element 501) (i.e. wherein the

step of calculating a first sequence of output values comprises performing a multiply-

accumulate operation utilizing each of the sum data elements).

8.   Regarding Claim 6, in addition to the elements stated above regarding claims 1

and 5, the output of the addition and subtraction (fig. 5 element 500) is applied to a data

rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output

is then applied to a product sum operation circuit (fig. 8 element 501) (i.e. wherein the

step of calculating a second sequence of output values comprises performing a

multiply-accumulate operation utilizing each of the difference data elements).

10.　　Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Uramoto (European Patent Application 0 506 111 A2) in view of ISO Standard 11172-3.

11.　　Regarding Claim 8, Uramoto discloses adder 22 adds the data i.e. (x0 + x7)

(page 8 lines 27 – 29) and subtractor 23 subtracts the data (x0 – x7) (page 8 lines 27 –

31) i.e.:

> a)　　calculating an array of sum data $S_{ADD}[k]$ according to
>
> $$S_{ADD}[k] = S[k] + S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$
>
> b)　　calculating an array of difference data $S_{SUB}[k]$ according to
>
> $$S_{SUB}[k] = S[k] - S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$

Uramoto does not disclose the rest of the claimed limitations in claim 8. ISO discloses

an inverse modified discrete cosine transform (page 36). ISO also discloses multiplying

samples by this function (page 41) i.e.

> c)　　calculating a first output audio data sample by a multiply-accumulate operation according to
>
> $$V[2i] = V[2i] + N[i, k]*S_{ADD}[k] \qquad \text{for } k = 0, 1, \ldots (m/2-1)$$
>
> $$\text{where } N[i, k] = \cos\left[\frac{(32+2i)(2k+1)\pi}{64}\right]$$
>
> d)　　calculating a second output audio data sample by a multiply-accumulate operation according to
>
> $$V[2i+1] = V[2i+1] + N[i, k]*S_{SUB}[k] \qquad \text{for } k = 0, 1, \ldots (m/2-1)$$
>
> $$\text{where } N[i, k] = \cos\left[\frac{(32+(2i+1))(2k+1)\pi}{64}\right]$$
>
> e)　　and repeating steps c) and d) for i = 0, 1, ... (n/2-1) to obtain a full set of output data.

It would have been obvious to one of ordinary skill in the art at the time of the invention

to use Uramoto's samples in ISO's decoder. It is merely one of many straightforward

implementations of decoding audio within ISO's decoder and does not involve the

excise of inventive skill.

12.   Regarding Claim 9, in addition to the elements stated above regarding claim 8,

ISO discloses any number of samples from 12 – 36 (page 36).

13.   Regarding Claim 10, in addition to the elements stated above regarding claims 8

and 9, ISO discloses decoding MPEG audio (page 41 and title).

14.   Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Sousa (European Patent Application 0 564 089 A1) in view of Uramoto (European

Patent Application 0 506 111 A2) and in further view of ISO Standard 11172-3.

10.   Regarding Claim 12, in addition to the elements stated above regarding claim 11,

ISO discloses the use of the inverse modified discrete cosine transform to decode audio

data (pages 36 and 41).

11.   Regarding Claim 13, in addition to the elements stated above regarding claims

11 and 12, ISO discloses decoding MPEG audio (page 41 and title).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Andrew C Flanders whose telephone number is (703)

305-0381. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Sinh Tran can be reached on (703) 305-4040. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SINH TRAN
SUPERVISORY PATENT EXAMINER

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